Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

CLAIMS

1-41. (Canceled).

42. (New) A method of altering a duty cycle of a first clock signal in an integrated circuit having a plurality of switches, comprising:

receiving, by at least a first portion of the switches, the first clock signal, wherein the first clock signal has a first pulse width;

in response to the first clock signal transitioning from a first logical state to a second logical state at time t:

gating a second portion of the switches to transition a second clock signal to the second logical state at substantially time t;

at substantially time t, propagating a signal in the first logical state through a delay element, wherein the delay element has a propagation delay time t1;

in response to the propagation delay time t1 being less than the first pulse width of the first clock signal, at substantially the end of time t + t1, gating a third portion of the switches to transition the signal to the second logical state; and

in response to the signal transitioning to the second logical state, at substantially the end of time t + t1, transitioning the second clock signal to the first logical state; and

in response to the clock signal transitioning from the second logical state to the first logical state at time t2:

gating a fourth portion of the switches such that the second clock signal is in the first logical state at substantially time t2;

at substantially time t2, propagating the signal in the second logical state through the delay element; and

in response to the propagation delay time t1 of the delay element being less than the first pulse width of the first clock signal, at substantially the end of time t2 + t1, gating a fifth portion of the switches such that the second clock signal does not transition to the second logical state at substantially the end of time t2 + t1.

43. (New) The method of Claim 42, further comprising:

in response to the propagation delay time t1 being equal to or greater than the pulse width of the first clock signal, gating a sixth portion of the switches such that the second clock signal transitions in substantial accordance with the first clock signal, such that the duty cycle of the first clock signal is substantially identical to a duty cycle of the second clock signal.

44. (New) The method of Claim 42, wherein the first portion of switches comprises four digital switches, wherein two digital switches are gated on and two digital switches are gated off in response to the first clock signal transitioning to the first logical state.

45. (New) The method of Claim 42, wherein the delay element comprises at least two delay blocks coupled in series, wherein each delay block inverts the signal.

46. (New) The method of Claim 45, wherein each delay block comprises at least a multiple of four NAND gates coupled in series.

47. (New) The method of Claim 42, wherein the integrated circuit is one of a pulse limiting circuit or a processor.

48. (New) The method of Claim 42, wherein the first logical state is a logical 1 and the second logical state is a logical 0.

49. (New) The method of Claim 42, wherein the second portion of switches comprises:

a first digital switch, also in the first portion, coupled to an inverter and a second digital switch, and gated on in response to the first clock signal being in the second logical state; and

the second digital switch coupled to a logical 1 power supply and to the first digital switch, and gated on in response to a portion of the third portion of switches being gated off, wherein in response to the first digital switch and second digital switch being gated on, the logical 1 power supply drives the second clock signal to the second logical state.

50. (New) The method of Claim 49, wherein the third portion of switches comprises:

a third digital switch coupled to the logical 1 power supply and a fourth digital switch, and gated by an inverse of the signal, wherein the third digital switch is gated on in response to the signal being in the first logical state;

the fourth digital switch coupled to the third digital switch and gated by the first clock signal, wherein the fourth digital switch is gated on in response to the first clock signal being in the second logical state; and

a fifth digital switch coupled to logical 0 ground and an inverter, and gated by the fourth digital switch, wherein the fifth digital switch is gated on and transitions the signal to the second logical state in response to the third and fourth digital switches being gated on.

51. (New) The method of Claim 42, wherein the step of transitioning the second clock signal to the first logical state comprises inverting the signal from the second logical state to the first logical state, thereby transitioning the second clock signal to the first logical state.

52. (New) The method of Claim 42, wherein the fourth portion of switches comprises a digital switch, also in the first portion, wherein the digital switch is gated on in response to the first clock signal being in the first logical state, the digital switch being coupled to a logical 0 ground and an inverter such that when gated on, the digital switch drives the second clock signal to the first logical state.

53. (New) The method of claim 50, wherein the fifth portion of switches comprises:

the third digital switch coupled to logical 1 voltage supply and gated by an inverse of the signal, wherein the third digital switch is gated off in response to the signal being in the second logical state;

the fourth digital switch coupled to the third digital switch and gated by the first clock signal, wherein the fourth digital switch is gated off in response to the first clock signal being in the first logical state;

the fifth digital switch coupled to logical 0 ground and gated by the fourth digital switch, wherein the fifth digital switch is gated off in response to the fourth digital switch being gated off;

a sixth digital switch, also in the first portion, coupled to an inverter and gated by the first clock signal, wherein the sixth digital switch is gated on in response to the first clock signal being in the second logical state;

a seventh digital switch coupled to a logical 1 power supply and the sixth digital switch, and gated by the fourth digital switch, wherein the seventh digital switch is gated on in response to the fourth digital switch being gated off; and

wherein in response to the sixth and seventh digital switches being gated on, the sixth digital switch maintains the second clock signal at the first logical state.

54. (New) An integrated circuit for altering a duty cycle of a first clock signal, the integrated circuit having a plurality of switches and comprising:

a first portion of the switches configured to receive the first clock signal, wherein the first clock signal has a first pulse width;

a second portion of the switches configured to transition a second clock signal to the second logical state at substantially time t, in response to the first clock signal transitioning from a first logical state to a second logical state at time t;

a delay element configured to propagate a signal in the first logical state at substantially time t, wherein the delay element has a propagation delay time t1;

a third portion of the switches configured to transition the signal to the second logical state, at substantially the end of time t + t1, in response to the propagation delay time t1 being less than the first pulse width of the first clock signal;

the second clock signal configured to transition to the first logical state in response to the signal transitioning to the second logical state at substantially the end of time t + t1;

a fourth portion of the switches configured to set the second clock signal in the first logical state at substantially time t2, in response to the clock signal transitioning from the second logical state to the first logical state at time t2;

the delay element further configured to propagate the signal in the second logical state at substantially time t2; and

a fifth portion of the switches configured to prevent the second clock signal from transitioning to the second logical state at substantially the end of time t2 + t1, in response to the propagation delay time t1 of the delay element being less than the first pulse width of the first clock signal.

55. (New) The integrated circuit of Claim 54, further comprising:

a sixth portion of the switches configured to transition the second clock signal in substantial accordance with the first clock signal, such that the duty cycle of the first clock signal is substantially identical to a duty cycle of the second clock signal, in response to the propagation delay time t1 being equal to or greater than the pulse width of the first clock signal.

56. (New) The integrated circuit of Claim 54, wherein the first portion of switches comprises four digital switches, wherein two digital switches are gated on and two digital switches are gated off in response to the first clock signal transitioning to the first logical state.

57. (New) The integrated circuit of Claim 54, wherein the delay element comprises at least two delay blocks coupled in series, wherein each delay block inverts the signal.

58. (New) The integrated circuit of Claim 57, wherein each delay block comprises at least a multiple of four NAND gates coupled in series.

59. (New) The integrated circuit of Claim 54, wherein the integrated circuit is one of a pulse limiting circuit or a processor.

60. (New) The integrated circuit of Claim 54, wherein the first logical state is a logical 1 and the second logical state is a logical 0.

61. (New) The integrated circuit of Claim 54, wherein the second portion of switches comprises:

a first digital switch, also in the first portion, coupled to an inverter and a second digital switch, and gated on in response to the first clock signal being in the second logical state; and

the second digital switch coupled to a logical 1 power supply and to the first digital switch, and gated on in response to a portion of the third portion of switches being gated off, wherein in

response to the first digital switch and second digital switch being gated on, the logical 1 power supply drives the second clock signal to the second logical state.

62. (New) The integrated circuit of Claim 61, wherein the third portion of switches comprises:

a third digital switch coupled to the logical 1 power supply and a fourth digital switch, and gated by an inverse of the signal, wherein the third digital switch is gated on in response to the signal being in the first logical state;

the fourth digital switch coupled to the third digital switch and gated by the first clock signal, wherein the fourth digital switch is gated on in response to the first clock signal being in the second logical state; and

a fifth digital switch coupled to logical 0 ground and an inverter, and gated by the fourth digital switch, wherein the fifth digital switch is gated on and transitions the signal to the second logical state in response to the third and fourth digital switches being gated on.

63. (New) The integrated circuit of Claim 54, wherein transitioning the second clock signal to the first logical state comprises inverting the signal from the second logical state to the first logical state, thereby transitioning the second clock signal to the first logical state.

64. (New) The integrated circuit of Claim 54, wherein the fourth portion of switches comprises a digital switch, also in the first portion, wherein the digital switch is gated on in response to the first clock signal being in the first logical state, the digital switch being coupled to a logical 0 ground and an inverter such that when gated on, the digital switch drives the second clock signal to the first logical state.

65. (New) The integrated circuit of claim 64, wherein the fifth portion of switches comprises:

the third digital switch coupled to logical 1 voltage supply and gated by an inverse of the signal, wherein the third digital switch is gated off in response to the signal being in the second logical state;

the fourth digital switch coupled to the third digital switch and gated by the first clock signal, wherein the fourth digital switch is gated off in response to the first clock signal being in the first logical state;

the fifth digital switch coupled to logical 0 ground and gated by the fourth digital switch, wherein the fifth digital switch is gated off in response to the fourth digital switch being gated off;

a sixth digital switch, also in the first portion, coupled to an inverter and gated by the first clock signal, wherein the sixth digital switch is gated on in response to the first clock signal being in the second logical state;

a seventh digital switch coupled to a logical 1 power supply and the sixth digital switch, and gated by the fourth digital switch, wherein the seventh digital switch is gated on in response to the fourth digital switch being gated off; and

wherein in response to the sixth and seventh digital switches being gated on, the sixth digital switch maintains the second clock signal at the first logical state.